Amendments to the Claims:

Please insert this listing of claims, which replaces all prior versions, and listings of claims in the application.

Listing of Claims:

1. (Original) A semiconductor device suitable for applications in an electrostatic discharge (ESD) protection circuit, comprising:
a semiconductor substrate;
a first well formed in the substrate;
a second well formed in the substrate; and
a first doped region formed in the second well,
wherein the first well, the second well, and the first doped region collectively form a parasitic bipolar junction transistor (BJT), and
wherein the first well is the collector of the BJT, the second well is the base of the BJT, and the first doped region is the emitter of the BJT.

2. (Original) The semiconductor device of claim 1, wherein the first well is n-type, the second well is p-type, the first doped region is n-type, and the parasitic BJT is an NPN BJT.

3. (Original) The semiconductor device of claim 1, wherein the first well is p-type, the second well is n-type, the first doped region is p-type, and the parasitic BJT is a PNP BJT.

4. (Original) The semiconductor device of claim 1, further comprising
a second doped region formed in the first well; and
a third doped region formed in the substrate,
wherein the second doped region and the first well are of a same type of conductivity, and the second doped region is a contact to the first well, and
wherein the third doped region and the second well are of a same type of conductivity, and the third doped region is a contact to the second well.

5. (Original) The semiconductor device of claim 4, further comprising an ESD detection circuit, wherein the first doped region is connectable to a power supply,
wherein the second doped region is connectable to a contact pad for receiving an ESD, and
wherein the third doped region is connectable to the ESD detection circuit coupled to the contact pad for detecting the ESD.

6. (Original) The semiconductor device of claim 5, wherein the ESD detection circuit provides a trigger current to the third doped region in an ESD event, and
wherein the trigger current triggers the parasitic BJT to conduct the ESD current from the second doped region to the first doped region or from the first doped region to the second doped region.

7. (Original) The semiconductor device of claim 5, wherein the BJT is an NPN BJT, and the power supply is ground.

8. (Original) The semiconductor device of claim 5, wherein the BJT is a PNP BJT, and the power supply is a positive supply voltage.

9. (Original) The semiconductor device of claim 5, further comprising a fourth doped region formed in the second well,
wherein the fourth doped region and the second well are of a same type of conductivity, wherein the fourth doped region is also a contact to the second well,
wherein the third doped region and the fourth doped region are spaced apart from each other, and
wherein the fourth doped region is connectable to the power supply.

10. (Original) The semiconductor device of claim 1, further comprising
a second doped region formed in the first well;
a third doped region formed in the substrate; and
a fourth doped region formed in the second well,

wherein the first, second, third, and fourth doped regions are electrically isolated from each other by a plurality of isolation regions.

11. (Original) The semiconductor device of claim 10, wherein the isolation regions are shallow trench isolations (STIs).

12. (Original) The semiconductor device of claim 10, wherein the isolation regions are local oxidation of silicon (LOCOS) regions.

13. (Original) The semiconductor device of claim 1, further comprising
a second doped region formed in the first well;
a third doped region formed in the substrate; and
a fourth doped region formed in the second well,
wherein the first, second, third, and fourth doped regions are electrically isolated from each other by a plurality of dummy gate structures.

14. (Original) The semiconductor device of claim 13, wherein the gates of the dummy gate structures are doped with both P^+ and N^+ dopants, wherein a portion of the gates proximate a p-type doped region is doped with P^+ dopant, and a portion of the gates proximate an n-type doped region is doped with N^+ dopant.

15. (Original) The semiconductor device of claim 1, further comprising a second doped region for receiving a trigger current or a trigger voltage in an ESD event, wherein a portion of the second doped region is formed in the first well, and another portion of the second doped region is formed in the second well, and wherein the trigger current or the trigger voltage triggers the BJT to discharge the ESD in the ESD event.

16. (Currently Amended) A semiconductor device suitable for applications in an electrostatic discharge (ESD) protection circuit, comprising:
a semiconductor substrate;

a first well formed in the substrate;
a second well formed in the substrate;
a third well formed in the substrate; and
a first doped region formed in the second well,
wherein the first well, the second well, and the first doped region collectively form a first parasitic bipolar junction transistor (BJT), and wherein the second well, the third well, and the first doped region collectively form a second parasitic BJT, and
wherein the first well is the collector of the first BJT, the third well is the collector of the second BJT, the second well is the base of both of the first and the second BJTs, and the first doped region is the emitter of both of the first and the second BJTs.

17. (Original) The semiconductor device of claim 16, wherein the first BJT and the second BJT are both NPN-BJTs.

18. (Original) The semiconductor device of claim 16, wherein the first BJT and the second BJT are both PNP BJTs.

19. (Currently Amended) The semiconductor device of claim 16, further comprising
a second doped region formed in the first well;
a third doped region formed in the third well;
a fourth doped region formed in the substrate; and
a fifth doped region formed in the substrate,
wherein the second doped region and the first well are of a same type of conductivity, and the second doped region is a contact to the first well,
wherein the third doped region and the third well are of a same type of conductivity, and the third doped region is a contact to the third well, and
wherein the fourth doped region, the fifth doped region, and the second well are of a same type of conductivity, wherein the fourth doped region and the fifth doped region are both contacts to the second well, and wherein the fourth doped region and the fifth doped region are spaced apart from each other.

20. (Original) The semiconductor device of claim 19,
wherein the first doped region is connectable to a power supply,
wherein the second and the third doped regions are connectable to a contact pad for receiving an ESD, and
wherein the fourth and fifth doped regions are connectable to an ESD detection circuit, wherein the ESD detection circuit is coupled to the contact pad for detecting the ESD.

21. (Original) The semiconductor device of claim 20, wherein the ESD detection circuit provides a trigger current or a trigger voltage to the fourth and fifth doped regions in an ESD event, wherein the trigger current or trigger voltage provided to the fourth doped region triggers the first BJT to conduct the ESD current from the second doped region to the first doped region or from the first doped region to the second doped region, and the trigger current or trigger voltage provided to the fifth doped region triggers the second BJT to conduct the ESD current from the third doped region to the first doped region or from the first doped region to the third doped region.

22. (Original) The semiconductor device of claim 19, wherein the first, second, third, fourth, and fifth doped regions are electrically isolated from each other.

23. (Original) The semiconductor device of claim 16, further comprising a plurality of dummy gate structure to electrically isolate at least two of the first, second, third, fourth, and fifth doped regions.

24. (Original) The semiconductor device of claim 23, wherein the gates of the dummy gate structures are doped with both P^+ and N^+ dopants, wherein a portion of the gates proximate a p-type doped region is doped with P^+ dopant, and a portion of the gates proximate an n-type doped region is doped with N^+ dopant.

25. (Original) The semiconductor device of claim 19, wherein a portion of the fourth doped region is formed in the first well, and another portion of the fourth doped region is formed in the second well, and wherein a portion of the fifth doped region is formed in the second well, and another portion of the fifth doped region is formed in the third well.

26. (Original) A semiconductor device suitable for applications in an electrostatic discharge (ESD) protection circuit, comprising:
a semiconductor substrate;
a first well formed in the substrate;
a second well formed in the substrate;
a third well formed in the substrate;
a first doped region formed in the second well; and
a second doped region formed in the second well,
wherein the first well, the second well, and the first doped region collectively form a first parasitic bipolar junction transistor (BJT), and the second well, the third well, and the second doped region collectively form a second parasitic BJT, and
wherein the first well is the emitter of the first BJT, the third well is the emitter of the second BJT, the second well is the base of both of the first and the second BJTs, the first doped region is the collector the first BJT, and the second doped region is the collector of the second BJT.

27. (Original) The semiconductor device of claim 26, further comprising
a third doped region formed in the substrate, wherein the third doped region is a contact to the first well;
a fourth doped region formed in the second well; and
a fifth doped region formed in the substrate, wherein the fifth doped region is a contact to the third well,
wherein the first and second doped regions are connectable to a contact pad for receiving an ESD in an ESD event, the third and fifth doped regions are connectable to a power supply, and the fourth doped region is connectable to an ESD detection circuit, wherein the ESD detection circuit is coupled to the contact pad for detecting the ESD.

28. (Original) The semiconductor device of claim 27, wherein a portion of the third doped region is formed in the first well, and another portion of the third doped region is formed in the second well, and wherein a portion of the fifth doped region is formed in the second well, and another portion of the fifth doped region is formed in the third well.

29. (Original) The semiconductor device of claim 27, wherein the ESD detection circuit triggers the first and second BJTs to conduct the ESD current from the first and second doped regions to the third and fifth doped regions, respectively, or from the third and fifth doped regions to the first and second doped regions, respectively.

30. (Original) The semiconductor device of claim 27, wherein the first doped region, the second doped region, the third doped region, the fourth doped region, and the fifth doped region are isolated from each other by a plurality of gate structures, wherein a first gate structure is formed between the first and third doped regions, and the first gate structure, the first doped region, the third doped region, and the second well form a first MOS transistor, wherein a second gate structure is formed between the second and fifth doped regions, and the second gate structure, the second doped region, the fifth doped region, and the second well form a second MOS transistor.

31. (Original) The semiconductor device of claim 30, wherein the first gate and the second gate are both connectable to the ESD detection circuit to trigger the first and second BJTs to discharge the ESD current in an ESD event.

32-36. (Canceled)